CofC

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent No. 6,894,556 B2	)	Serial No. 10/760,474
Inventor(s): Atsushi KAWASUMI	)	Filed: January 21, 2004
Issue Date: May 17, 2005	)	Attorney Docket No. 005405.00008

For: CURRENT MIRROR CIRCUIT AND CURRENT SOURCE CIRCUIT

REQUEST FOR CERTIFICATE OF CORRECTION

U.S. Patent and Trademark Office
Customer Service Window
Randolph Building, Mail Stop: Certificate of Correction Branch
401 Dulany Street
Alexandria, VA 22314

Sir:

Pursuant to 35 U.S.C. § 254 and 37 C.F.R. § 1.322, this is a request for the issuance of a Certificate of Correction in the above-identified patent. Two (2) copies of PTO Form 1050 are appended. The complete Certificate of Correction involves one page.

The mistakes identified in the appended Form occurred through no fault of the Applicant, as clearly disclosed by the records of the application, which matured into this patent. Enclosed for your convenience is the relevant portion of the Amendment filed November 19, 2004.

Issuance of the Certificate of Correction containing the corrections is respectfully requested. Since these changes are necessitated through no fault of the Applicants, no fee is believed to be associated with this request. Nonetheless, should the Patent and Trademark Office determine that a fee is required, please charge our Deposit Account No. 19-0733.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Dated: November 18, 2005

By: _____
Christopher R. Glembocki
Registration No. 38,800

1001 G Street, N.W. (11th Fl.)
Washington, D.C. 20001
(202) 824-3000

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: 6,894,556 B2

DATED: May 17, 2005

INVENTOR(S): Atsushi KAWASUMI

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Column 10, Claim 1, Line 8:
Please replace "$V_{g1\text{-}kVd1}$" with --V_{g1}-kV_{d1}--

In Column 11, Claim 24, Line 4:
Please replace "PMQS" with --PMOS--

Mailing Address of Sender:

Banner & Witcoff, Ltd.
11th Floor
1001 G Street, N.W.
Washington, DC 20001-4597

FORM PTO 1050 (Rev.2-93)

U.S. PAT. NO

No. of add'l copies
@ $0.50 per page

☐

NOV 29 2005

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: 6,894,556 B2

DATED: May 17, 2005

INVENTOR(S): Atsushi KAWASUMI

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Column 10, Claim 1, Line 8:
Please replace "$V_{g1\text{-}kVd1}$" with --V_{g1}-kV_{d1}--

In Column 11, Claim 24, Line 4:
Please replace "PMQS" with --PMOS--

Mailing Address of Sender:

Banner & Witcoff, Ltd.
11th Floor
1001 G Street, N.W.
Washington, DC 20001-4597

FORM PTO 1050 (Rev.2-93)

U.S. PAT. NO

No. of add'l copies
@ $0.50 per page

☐

NOV 2 9 2005

****
*** TX REPORT ***
****

TRANSMISSION OK

TX/RX NO	3485
RECIPIENT ADDRESS	0340#099999#99999#17038729306#
DESTINATION ID	
ST. TIME	11/19 11:40
TIME USE	01'41
PAGES SENT	6
RESULT	OK

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application Of	)	
	)	Group Art Unit: 2816
Atsushi Kawasumi	)	
	)	Examiner: T. Cunningham
Serial No.: 10/760,474	)	
	)	
Filed: January 21, 2004	)	Confirmation No. 9799
	)	
For: Current Mirror Circuit And Current Source Circuit	)	Atty. Dkt. No. 005405.00008
	)	

U.S. Patent and Trademark Office
220 20th Street S.
Customer Window
Crystal Plaza Two, Lobby, Room 1B03
Arlington, VA 22202

This paper of 6 pages is being transmitted to 703 872 9306 on November 19, 2004.

Christopher R. Glembocki
Reg. No. 38,800

Sir:

Amendment

This paper is a resubmission of the Amendment of September 20, 2004, in response to the Notice of Non-Compliant Amendment of November 10, 2004. In particular, the label of claim 22 has been corrected. The drawing correction was previously submitted so it is not being submitted again.

In response to the non-final Office Action mailed May 19, 2004, please amend the application as follows.

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application Of	)	
	)	Group Art Unit: 2816
Atsushi Kawasumi	)	
	)	Examiner: T. Cunningham
Serial No.: 10/760,474	)	
	)	
Filed: January 21, 2004	)	Confirmation No. 9799
	)	
For: Current Mirror Circuit And Current Source Circuit	)	Atty. Dkt. No. 005405.00008
	)	

U.S. Patent and Trademark Office
220 20th Street S.
Customer Window
Crystal Plaza Two, Lobby, Room 1B03
Arlington, VA 22202

This paper of 6 pages is being transmitted to 703 872 9306 on November 19, 2004.

Christopher R. Glembocki
Reg. No. 38,800

Sir:

Amendment

This paper is a resubmission of the Amendment of September 20, 2004, in response to the Notice of Non-Compliant Amendment of November 10, 2004. In particular, the label of claim 22 has been corrected. The drawing correction was previously submitted so it is not being submitted again.

In response to the non-final Office Action mailed May 19, 2004, please amend the application as follows.

Amendments to the Claims are reflected in the Listing of Claims, which begins on page 2 of this paper.

Remarks begin on page 4 of this paper.

The listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claims 1-21 (Previously Cancelled).

22. (Previously Presented) A current source circuit comprising:

a first PMOS transistor having a source coupled to a first power source, a gate receiving a voltage from a voltage circuit, and a drain coupled to a node; and

a compensation circuit comprising;

more than one compensation PMOS transistors, each compensation PMOS transistor having a gate, a source coupled to the first power source, and a drain coupled to the node; and

more than one subtracter, each subtracter coupled to the gate of each compensation PMOS transistor, each subtracter configured to supply voltage expressed by arithmetic series a_k to the gate of each compensation PMOS transistor,

where the a_k is the arithmetic series equal to :

$V_{gl}-kV_{dl}$ (k=1, 2, . . ., n),

V_{dl} is the drain-source voltage of the first transistor,

V_{gl} is the gate-source voltage of the first transistor, and

n is the number of the PMOS transistors of the compensation circuit.

23. (Currently Amended) A current source circuit comprising:

a first PMOS transistor group having at least two PMOS transistors connected in series, the first PMOS transistor group including:

a first PMOS transistor having a source coupled to a first power source, a gate receiving a first voltage provided by a voltage circuit, and a drain, wherein the first PMOS transistor is defined as being the electrically closest to the first power source,

a second PMOS transistor having a source, a gate receiving a second voltage provided by ~~a~~ the voltage circuit, and a drain wherein the drain of the second PMOS transistor coupled to a node, wherein the last PMOS transistors is defined as being the electrically furthest from the first power source; and

a compensation circuit comprising a second PMOS transistor group having at least two PMOS transistors connected in series, the second PMOS transistor group including:

a third PMOS transistor having a gate, a source, and a drain, wherein the source of the third PMOS transistor is coupled to the first power source, wherein the third PMOS transistor is defined as being the electrically closest to the first power source in the second PMOS transistor group, and

a fourth PMOS transistor having a gate, a source, and a drain, wherein the drain of the fourth PMOS transistor is coupled to the node, wherein the fourth PMOS transistor is defined as being the electrically furthest from the first power source in the second transistor group; and

the group of subtracters, each subtracter, including:

a first subtracter coupled to a gate of the third PMOS transistor, the first subtracter configured to supply difference voltages, being a difference between gate-source voltages and drain-source voltage of the first PMOS transistor, to the gate source of the third PMOS transistor;

a second subtracter coupled to a gate of the fourth PMOS transistor, the second subtracter configured to supply difference voltages, being a difference between gate-source voltages and drain-source voltage of the second PMOS transistor, to the gate source of the third PMOS transistor.

24. (New) A current source circuit comprising:

a first PMOS transistor group having at least two PMOS transistors connected in series, the first PMOS transistor group including:

a first PMOS transistor having a source coupled to a first power source, a gate receiving a first voltage provided by a first voltage circuit, and a drain, wherein the first PMOS transistor is defined as being the electrically closest to the first power source,

a second PMOS transistor having a source, a gate receiving a second voltage provided by a second voltage circuit, and a drain wherein the drain of the second PMOS transistor coupled to a node, wherein the last PMOS transistors is defined as being the electrically furthest from the first power source; and

a compensation circuit comprising a second PMOS transistor group having at least two PMOS transistors connected in series, the second PMOS transistor group including:

a third PMOS transistor having a gate, a source, and a drain, wherein the source of the third PMOS transistor is coupled to the first power source, wherein the third PMOS transistor is defined as